

MP3 Decoder Adapter

VSI011 Adapter Board for SPI and I2C Bus

Datasheet Rev.: 1.0.
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Features

- VLSI **VS1011E** MP3/WAV Decoder
- Decodes MPEG 1 & 2 audio layer 3 (ISO 11172-3), WAV and PCM files
- Supports VBR (variable bitrate) for MP3
- Stream support
- High-quality stereo DAC with no phase error between channels
- Stereo earphone driver capable of driving a 300ohm load
- Onboard Level Shifter for 5V Operation
- Host Microcontroller Interface via SPI and I2C
- Operating Voltage: 5VDC

Ordering Information

Art.-No. 01.0035

MP3 Adapter Board

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Specifications

DECODER

Type	VLSI VS1011E
Clock	12.288 MHz
Decoded Audio Formats	MPEG 1 & 2 audio layer 3 (ISO 11172-3), WAV and PCM

AUDIO

DAC Resolution	16 bits
THD	0.1%
Dynamic Range	88dB
Output Voltage	1.6...2.1VPP @ 30 Ohms

INTERFACE

SPI	4-Wire Interface, max. 2MHz clock
I2C	Control of DCS signal via DAC
Interrupt	Open-drain interrupt output
Reset	Low active reset input

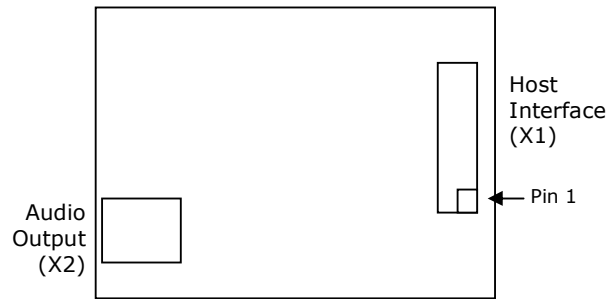
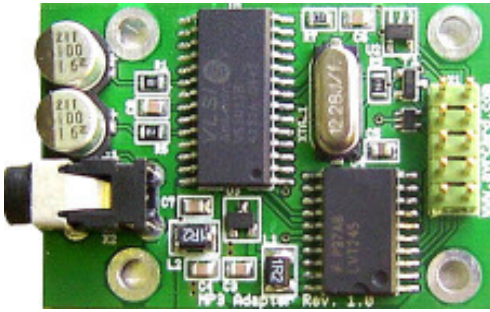
Power Supply

Requirement	5 VDC, max. 45mA
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Mechanical

Size (L x W)	47 x 32 mm
Weight	20 g

Connector Specifications



Host Interface Connector

X1: Host Interface			
No.	Signal	Type ¹	Function
1	+5V	POWER	Supply power
2	CS	IN	SPI Bus
3	SCK	IN	
4	MOSI	IN	
5	MISO	OUT ²	
6	GND	POWER	Ground
7	RESET	IN	VS1011 reset signal, active low
8	INT	OUT ³	VS1011 DREQ signal, active low
9	SCL	IN	I2C Bus
10	SDA	IN/OUT	

¹ Direction is indicated with respect to the adapter module.

² Output is tristated when CS is deasserted.

³ Open-drain output, external pull-up resistor required.

Application Information

Host Interface Setup

The MP3 Adapter is operated through the following interfaces:

- SPI (Adapter has slave function with MISO, MOSI, SCK, CS signals)
- I2C for controlling the DCS signal on the VS1011 (Adapter has slave function with SDA, SCL signals)
- DREQ line of VS1011 is connected to the Interrupt output line via a FET. The DREQ signal is therefore inverted.

Place a pull-up resistor on the interrupt line.

Controlling the DCS signal of VS1011

The MP3 Adapter module has been designed for a host interface with standard 4-line SPI and I2C interfaces. As the VS1011 has two chip selects, the second select line is controlled by a small inexpensive 6-bit DAC (MAX5362) via I2C.

The I2C slave address of the MAX5362 is %0110000.

- To assert the DCS signal, send the value 0x00 to the DAC via I2C write command.
- To deassert the DCS signal, send the value 0xFC to the DAC via I2C write command.

Writing VS1011 register values

The VS1011 registers can be accessed over the SPI, controlled by the CS signal. Each register is one word (16 bits) wide. Please refer to the VS1011 datasheet for a complete description of the registers.

Following pseudocode shows how to access the registers:

```
Assert CS
Issue VS1011 write command: send 0x02 to SPI
Wait for data to be sent
Send register address to SPI
Wait for data to be sent
Send high byte of register value to SPI
Wait for data to be sent
Send low byte of register value to SPI
Wait for data to be sent
Deassert CS
Delay 5 microseconds after sending data
```

VS1011 Inizialization Procedure

The shaded paragraphs refer to VS1011 registers. Please see VS1011 datasheet for register addresses and access information.

Initialize Host Interface Ports

1. Set CS (MP3/ChipSelect) as output
2. Set MOSI as output
3. Set SCK as output
4. Set SCK to low level
5. Set SPI clock speed to 2 MHz
6. Select clock phase positive going in middle of data
7. Set SPI to master mode
8. Set I2C to master mode, clock speed to 100kHz

Hardware reset of VS1011

1. Assert VS1011 reset
2. Delay 30ms
3. Deassert CS by setting to high level
4. Deassert DCS
`write the value 0xFC to the MAX5362 DAC`
5. Release VS1011 Reset
6. Delay 10ms (2.5ms according to datasheet)
7. Set volume to minimum:
`VOL <- 0xFFFF`
8. Set CLOCKF to compensate for a 24.576 MHz x-tal. Activate clock doubler. The value should be $f_{\text{Clock}}/2000$. The values shown are for the 12.288MHz crystal on the MP3 adapter board.
`CLOCKF <- 6144 + 0x8000`
9. Delay 1 ms
10. Wait for DREQ
11. Set slow sample rate for slow analog part startup
`AUDATA <- 10 // 10 Hz`
12. Delay 100 ms
13. Switch on the analog parts
`VOL <- 0xFEFE`
`AUDATA <- 44101 // 44.1kHz stereo`
`VOL <- 0x2020 // or other default value`

Software Reset of VS1011

1. Delay 200ms
2. Set SW reset bit, set VS10xx native mode on SPI, allow tests (e.g. sine tests)
`MODE <- SM_RESET + SM_SETTOZERO3 + SM_SDINEN + SM_TESTS`
3. Delay 2us
4. Rewrite SCI_CLOCKF after soft reset
`CLOCKF <- 6144 + 0x8000`
5. Send 1024 nulls
Assert DCS
Send 0x53 to SPI

```
repeat
  Wait for DREQ
  Send 0x00 to SPI
  Wait for data to be sent to SPI
Until 1024 bytes are done
Deassert DCS
```

Playing MP3 Data

Before playing a new MP3 stream, perform a software reset on the VS1011.

Below is an example pseudocode for playing a stream of MP3 data by reading blocks of data from a mass storage device and sending them to the VS1011.

```
Software reset VS1011
Open storage file for reading
For each data block do
  Read one data block of mp3 data
  For each 32 bytes in the data block do
    wait for DREQ
    Assert DCS
    Repeat
      Send next byte to SPI
      Wait until data byte was sent
    Until 32 bytes are done
    Deassert DCS
  Endfor
Endfor
Close File
```

Notice to Users

The intended use of the MP3 Adapter modules is described in this document. Other than the described uses are not permitted or only after consultation with the manufacturer.

MP3 Adapter modules are not authorized for use as critical components in life-support devices or systems.

Life-support devices or systems are devices or systems intended for surgical implantation into the body or to sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling and user's manual, can be reasonably expected to result in significant injury.

No complex software or hardware system is perfect. Bugs are always present in a system of any size. In order to prevent danger to life or property, it is the responsibility of the system designer to incorporate redundant protective mechanisms appropriate to the risk involved.

All MP3 Adapter modules are 100 percent functionally tested. Additional testing may include visual quality control inspections. Specifications are based on characterization of tested sample units rather than testing over temperature and voltage of each unit. MP3 Adapter modules may qualify components to operate within a range of parameters that is different from the manufacturer's recommended range.