

MP3orator

Embedded Digital Audio Player

Datasheet Rev.: 1.0
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Features

- Atmel **ATmega644** RISC CPU @ 6MHz
- VLSI **VS1011E** MP3/WAV Decoder
- Decodes MPEG 1 & 2 audio layer 3 (ISO 11172-3), WAV and PCM files
- Supports VBR (variable bitrate) for MP3
- High-quality stereo DAC with no phase error between channels
- Stereo earphone driver capable of driving a 30Ohm load
- **Sdcard** removable storage device, on SPI
- Remote controlled via UART, I2C and/or keyboard
- Operating Voltage: 3.3VDC

Ordering Information

Art.-No. 01.0138
MP3orator, OEM board

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Specifications

AUDIO

Decoder Type	VLSI VS1011E
Clock	12.288 MHz
Decoded Audio Formats	MPEG 1 & 2 audio layer 3 (ISO 11172-3), WAV and PCM
DAC Resolution	16 bits
THD	0.1%
Dynamic Range	88dB
Output Voltage	1.6...2.1VPP @ 30 Ohms

CPU

Type	Atmel ATmega644 8-bit RISC
Clock	6 MHz

STORAGE DEVICE

Type	SDcard
Operating Mode	SPI

I/O

Serial	UART with TXD, RXD
Two-wire	I2C with SDA, SCL
Parallel	12 I/O Ports, freely assignable

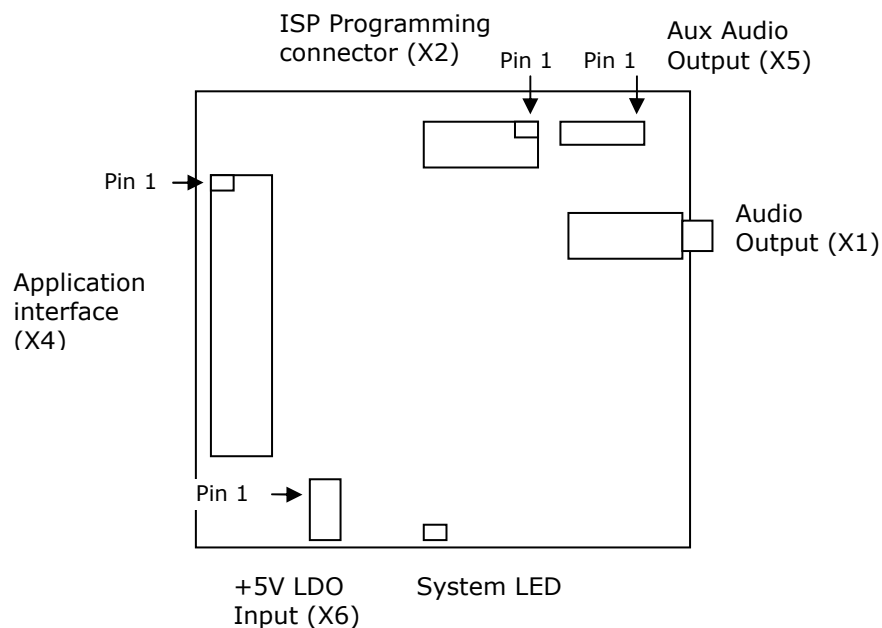
Power Supply

Requirement	3.3V or 5VDC, max. 40mA
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Mechanical

Size (L x W)	46 x 48.5 mm
Weight	30 g

Connector Specifications



Application Interface

X4: Application			
No.	Signal	Type	Description
1	+3.3V	POWER	DC Input voltage, 3.3V, or output voltage when LDO is used
2	TXD	OUT	UART Serial Interface, transmit data
3	RXD	IN	UART Serial Interface, receive data
4	SHIFT	IN	SHIFT signal (alternatively used for I2C Interface, clock)
5	nBUSY	OUT	BUSY signal, active low (alternatively used for I2C interface, data)
6	GND	POWER	Ground
7	PD4	IN/OUT	I/O Port
8	PD5	IN/OUT	I/O Port
9	PD6	IN/OUT	I/O Port
10	PD7	IN/OUT	I/O Port
11	PA0	IN/OUT	I/O Port / ADC Input
12	PA1	IN/OUT	I/O Port / ADC Input
13	PA2	IN/OUT	I/O Port / ADC Input
14	PA3	IN/OUT	I/O Port / ADC Input
15	PA4	IN/OUT	I/O Port / ADC Input
16	PA5	IN/OUT	I/O Port / ADC Input
17	PA6	IN/OUT	I/O Port / ADC Input
18	PA7	IN/OUT	I/O Port / ADC Input
19	nRES	IN/OUT	CPU Reset, active low
20	(N.C.)		No Connection

Audio

X5: Aux Audio			
No.	Signal	Type	Description
1	AGND	POWER	Audio Signal Ground
2	RIGHT	OUT	Right channel audio output
3	LEFT	OUT	Left channel audio output

ISP Programming Interface

X1: Programming			
No.	Signal	Type	Description
1	MISO	OUT	SPI bus
2	+3.3V	POWER	Digital power
3	SCK	IN	SPI bus
4	MOSI	IN	
5	RESET	IN	CPU Reset Input/Output
6	GND	RESET	Signal and power ground

Device Operation

Power Supply

The MP3orator module can be powered either from

- a) a regulated 5VDC source through X6, or
- b) a regulated 3.3VDC source, through X4. In this case, X6 must be disconnected.

Signal Levels

All signal levels present on the Application Interface connector X4 are 3.3V logic levels.

A 100 Ohm series resistor is present on each I/O line to provide a minimum protection against ESD. If long wires are connected, or if other signal levels are to be applied, additional signal conditioning circuitry is required.

Programming Guidelines

CPU Port Assignments

Port	Function	In/Out	Assigned to	Target
PA0	ADC0	In/ Out	Application Interface X4	X4.11
PA1	ADC1	In/ Out		X4.12
PA2	ADC2	In/ Out		X4.13
PA3	ADC3	In/ Out		X4.14
PA4	ADC4	In/ Out		X4.15
PA5	ADC5	In/ Out		X4.16
PA6	ADC6	In/ Out		X4.17
PA7	ADC7	In/ Out		X4.18
PB0	XCK	Out	VS1011 Decoder	CS
PB1	T1	Out		DCS
PB2	AIN0	Out		Reset
PB3	AIN1			
PB4	SS	Out	SDcard	CS
PB5	MOSI	Out	Sdcard, VS1011	SDI, SI
PB6	MISO	In		SDO, SO
PB7	SCK	Out		SCK
PC0	SCL	In/Out		Application Interface X4
PC1	SDA	In/Out	X4.5	
PC2	TCK			
PC3	TMS			
PC4	TDO			
PC5	TDI	Out	System LED	
PC6	TOSC1	In	SDcard	Card Detect
PC7	TOSC2	In		Write Protect
PD0	RXD	In	Serial Interface	X4.2
PD1	TXD	Out		X4.3
PD2	INT0	In	VS1011	DREQ
PD3	INT1			
PD4	OC1B			
PD5	OC1A			
PD6	ICP			
PD7	OC2			

Writing VS1011 register values

The VS1011 registers can be accessed over the SPI, controlled by the CS signal. Each register is one word (16 bits) wide. Please refer to the VS1011 datasheet for a complete description of the registers.

Following pseudocode shows how to access the registers:

```
Assert CS
Issue VS1011 write command: send 0x02 to SPI
Wait for data to be sent
Send register address to SPI
Wait for data to be sent
Send high byte of register value to SPI
Wait for data to be sent
Send low byte of register value to SPI
Wait for data to be sent
Deassert CS
Delay 5 microseconds after sending data
```

VS1011 Initialization Procedure

The shaded paragraphs refer to VS1011 registers. Please see VS1011 datasheet for register addresses and access information.

Initialize Host Interface Ports

1. Set CS (MP3/ChipSelect) as output
2. Set MOSI as output
3. Set SCK as output
4. Set SCK to low level
5. Set SPI clock speed to 2 MHz
6. Select clock phase positive going in middle of data
7. Set SPI to master mode

Hardware reset of VS1011

1. Assert VS1011 reset
2. Delay 30ms
3. Deassert CS by setting to high level
4. Deassert DCS by setting to high level
5. Release VS1011 Reset
6. Delay 10ms (2.5ms according to datasheet)
7. Set volume to minimum:

```
VOL <- 0xFFFF
```

8. Set CLOCKF to compensate for a 24.576 MHz x-tal. Activate clock doubler. The value should be $f_{\text{Clock}}/2000$. The values shown are for the 12.288MHz crystal on the MP3 adapter board.

```
CLOCKF <- 6144 + 0x8000
```

9. Delay 1 ms
10. Wait for DREQ
11. Set slow sample rate for slow analog part startup

```
AUDATA <- 10 // 10 Hz
```

12. Delay 100 ms
13. Switch on the analog parts

```
VOL <- 0xFEFE
```

```
AUDATA <- 44101 // 44.1kHz stereo
VOL <- 0x2020 // or other default value
```

Software Reset of VS1011

1. Delay 200ms
2. Set SW reset bit, set VS10xx native mode on SPI, allow tests (e.g. sine tests)

```
MODE <- SM_RESET + SM_SETTOZERO3 + SM_SDINNEW + SM_TESTS
```

3. Delay 2us
4. Rewrite SCI_CLOCKF after soft reset

```
CLOCKF <- 6144 + 0x8000
```

5. Send 1024 nulls

```
Assert DCS
Send 0x53 to SPI
repeat
    Wait for DREQ
    Send 0x00 to SPI
    Wait for data to be sent to SPI
Until 1024 bytes are done
Deassert DCS
```

Playing MP3 Data

Before playing a new MP3 stream, perform a software reset on the VS1011.

Below is an example pseudocode for playing a stream of MP3 data by reading blocks of data from a mass storage device and sending them to the VS1011.

```
Software reset VS1011
Open storage file for reading
For each data block do
    Read one data block of mp3 data
    For each 32 bytes in the data block do
        wait for DREQ
        Assert DCS
        Repeat
            Send next byte to SPI
            Wait until data byte was sent
        Until 32 bytes are done
        Deassert DCS
    Endfor
Endfor
Close File
```

Appendix

Notice to Users

The intended use of the MP3orator modules is described in this document. Other than the described uses are not permitted or only after consultation with the manufacturer.

MP3orator modules are not authorized for use as critical components in life-support devices or systems.

Life-support devices or systems are devices or systems intended for surgical implantation into the body or to sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling and user's manual, can be reasonably expected to result in significant injury.

No complex software or hardware system is perfect. Bugs are always present in a system of any size. In order to prevent danger to life or property, it is the responsibility of the system designer to incorporate redundant protective mechanisms appropriate to the risk involved.

All MP3orator modules are 100 percent functionally tested. Additional testing may include visual quality control inspections. Specifications are based on characterization of tested sample units rather than testing over temperature and voltage of each unit. MP3orator modules may qualify components to operate within a range of parameters that is different from the manufacturer's recommended range.

Revision History

Rev. 1.0., Date: 12.10.2006
Initial release.

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